

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. Miyamoto et al. : Art Unit:
Serial No.: To Be Assigned : Examiner:
Filed: Herewith :
FOR: ASYNCHRONOUS FIFO :
CIRCUIT AND METHOD OF READING :
AND WRITING DATA THROUGH
ASYNCHRONOUS FIFO CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R :

Prior to examination, please amend the above-identified application as follows:

SPECIFICATION:

Specification at page 4, line 13:

One aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 5, line 10:

Another aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 7, line 3:

Still another aspect of the present invention is the asynchronous FIFO circuit, wherein said error write counter and said error read counter are formed of a gray code counter.

Specification at page 7, line 7:

Yet still another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

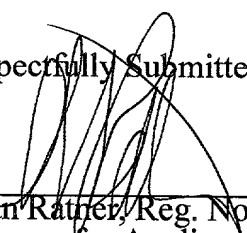
Specification at page 8, line 1:

Still yet another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Specification at page 9, line 20:

A further aspect of the present invention is the asynchronous FIFO data reading and writing method, wherein said error write step and said error read step are formed of a gray code count step.

Respectfully Submitted,


Allan Ratner, Reg. No. 19,717
Attorney for Applicants

AR/dlm

Enclosures: Version with markings to show changes made

Suite 301
One Westlakes, Berwyn
P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. 18-0350 of any fees associated with this communication.

EXPRESS MAIL Mailing Label Number: EL 923263910 US

Date of Deposit: December 4, 2001

I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.



Kathleen Libby

10006960 120401

VERSION WITH MARKINGS TO SHOW CHANGES MADE

SPECIFICATION:

Specification at page 4, line 13:

~~The 1st invention~~ One aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 5, line 10:

~~The 2nd invention~~ Another aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 7, line 3:

~~The 3rd invention~~ Still another aspect of the present invention is the asynchronous FIFO circuit ~~according to 1st or 2nd inventions~~, wherein said error write counter and said error read counter are formed of a gray code counter.

Specification at page 7, line 7:

~~The 4th invention~~ Yet still another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Specification at page 8, line 1:

~~The 5th invention~~ Still yet another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Specification at page 9, line 20:

~~The 6th invention~~ A further aspect of the present invention is the asynchronous FIFO data reading and writing method ~~according to 4th or 5th inventions~~, wherein said error write step and said error read step are formed of a gray code count step.

10006880-120001